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Appl. No. 10/773,673 Amdt. dated September 24, 2008 Reply to Office Action of June 23, 2008

## Amendments to the Specification:

Please change the title from "METHODS AND APPARATUS FOR GENERAL DEFERRED EXECUTION PROCESSORS" to "METHODS AND APPARATUS FOR STORING EXPANDED WIDTH INSTRUCTIONS IN A VLIW MEMORY FOR DEFERRED EXECUTION".

Please replace the paragraph beginning at page 21, line 16, with the following rewritten paragraph:

Fig. 12 illustrates aspects of a DXP2 processor including a VIM Basket 1210, local instruction registers IR1 1212 and IR2 1214, and decode 1216 and execution 1218 stages in a PE. Some of the differences between the Fig. 12 organization and the SLAMDunk1 organization shown in Fig. 5 are as follows: The VIMBasket 1210 consists of either four slots 1243-1244 or six slots 1244-1243 in Fig. 12 instead of the fixed five slot arrangement in Fig. 5. Two instruction widths are supported in the DXP2 of Fig. 12, a 64-bit instruction type and a 32-bit instruction type, for example 1220 and 1222 are 64-bit instructions and 1224 and 1226 are 32-bit instructions. A 3-bit UAF field 1230 is used to support the six execution units. A new tag field t 1232 is specified for future use. A second memory 1236 for RFI control parameter storage may be accessed in parallel with a VIMBasket 1210 access. No Short Instruction Word (SIW) path bypassing the VIMB is used in the DXP2 since this capability can be obtained through use of the XV's enable bits.